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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/045,507	03/20/1998	DONALD MALCOLM MACINTYRE	MAI1003	1010

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EXAMINER
WILLE, DOUGLAS A

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 07/25/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/045,507	MACINTYRE, DONALD MALCOLM
	Examiner	Art Unit
	Douglas A Wille	2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 May 2002*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *59-67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *59-67* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a)☐ The translation of the foreign language provisional application has been received.

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s).

5)☐ Other

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 59 – 67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kata et al. in view of Lin, Tsukamoto, Igarashi et al. and Feldner et al.

1. With respect to claim 59, Kata et al. show a wafer scale device (see Figures 3 and 4 and column 6, line 36 et seq.) where the wafer is connected through film 64 to bumps 70. Lin shows a flip chip device (see Figure 5 and column 5, line 15) with a semiconductor chip 12 attached to an interposer board 22. Lin shows the interposer board attached to a PC board with layer of adhesive 36 but does not show a similar attachment between 12 and 22, noting that while it is standard practice (column 2, line 22) it prevents rework. Note that if rework is not as issue, bonding is recommended. Lin also teaches that the thermal coefficient of expansion of the interposer should match that of the die (column 6, line 28). Lin shows vias 24 in the plate 22 with evaporated traces 26 (column 6, line 64) on the plate which connects contacts 16 to vias 24 and solder beads 32 are formed on the surface of 22. Lin shows that the metallization 26 can be evaporated and if performed after forming the hole it will extend into the holes. In addition a conductive fill is used for the vias (column 6, line 66). Lin does not specify the material of the

match the CTE of the die. Lin shows that the claimed structure with a solid interposer has an advantage over other techniques since it permits testing (column 2, line 2). Igarashi et al. show the use of polyimide to bond the die to the intermediate sheet. Igarishi et al. teach to provide a bonding layer between the chip and the substrate to prevent the formation of a void which could damage the device (column 9, line 64). It would have been obvious to modify the device of Lin to include the glass ceramic plate taught by Tsukamoto to match the TCE of the die and plate and to use the polyimide bond taught by Igarashi et al. to have a known bonding material. It would have been obvious to use the Lin, Tsukamoto and Igarashi et al. technique on the Kata structure to provide a more robust interconnect structure which is testable. The above references do not show a unitary glass layer but Feldner et al. show (see abstract and column 4, line 66) a semiconductor wafer with a unitary glass layer with filled vias and the wafer is diced after the processing is complete. It would have been obvious to apply the Feldner et al. technique to provide a simpler processing method since all the processing is completed before separation.

3. With respect to claim 60, Lin teaches that the thermal coefficient of expansion of the interposer should match that of the die (column 6, line 28).

4. With respect to claim 61, Kata et al. do not specify that the wafer is silicon but it would be obvious to apply the structure to silicon; however, Lin shows specifically that the chip is silicon (column 6, line 32)

5. With respect to claims 62 and 63, Kata et al. do not disclose the material of pads 11 but since Al is used for the interconnect layer 60 and since Al is a well known connection material for Si, it would have been obvious to use Al for the pads. Note that the pad is also the same as

6. With respect to claim 64, since Lin shows that the vias can be filled by screen printing, it would have been obvious to use a conductive polymer as a design alternative since it lends itself to such a process.

7. With respect to claim 65, Kata et al. show a coating film on the surface that defined the ball contact (see cover Figure).

8. With respect to claim 66, Kata et al. show the conductor is a plug.

9. With respect to claim 67, Lin shows that the metallization 26 can be evaporated and if performed after forming the hole it will extend into the holes and will, in effect, have tow parts, one at the edge of the hole and the other extending into the hole.

Response to Arguments

2. Applicant states that the references do not show a glass sheet that is the same size as the wafer but note that Kata et al. show that the film 64 cover the wafer and with the interposer of Lin substituted for the film, the interposer would cover the whole wafer and would be glass as shown by Tsukamoto.

3. Applicant states that the references do not show an interconnect structure "as recited in Applicant's new independent claims. What interconnect structure is this? Note however, that Kata connection structure is the same as that claimed, except for the glass plate (which is show by Lin and Tsukamoto).

4. Applicant states that Lin does not show a wafer level device, which is true, but this is piecemeal analysis and the claimed structure is shown by the references taken as a whole.

5. Applicant states that there is no adhesive between the interposer and the chip 12 in the

teaches to provide an adhesive when rework is not considered. Note also that Igarishi et al. teach to provide a bonding layer between the chip and the substrate to prevent the formation of a void which could damage the device.

6. Applicant states that Tsukamoto does not show an adhesive but again, this is piecemeal analysis and Tsukamoto is not relied upon to show an adhesive but is relied upon to show the substrate material, which is independent of the use of an adhesive.

7. Applicant states that Igarishi et al. show the polyimide resin "encapsulates" the die and is this not compatible with a wafer scale layer that is recited. First, in Igaishi et al. the polyimide does not encapsulate the device, but fills the void between the chip and the carrier and will still function as an adhesive. Second, there is no reason why the Igarishi et al. resin could not be applied to a wafer scale device and the same process that inserts the polyimide in the Igarishi et al. device would be used to insert the material in a wafer scale device.

8. Applicant states that Feldner et al. addresses a chip scale device but Feldner et al. clearly states that a wafer is being referred to (column 4, line 50).

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas A Wille whose telephone number is (703) 308-4949. The examiner can normally be reached on M-F (6:15-3:45)

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

daw
July 16, 2002